Notice of Allowability	Application No.	Applicant(s)	
	10/671,745	ISHIGUCHI, KAZUHIRO	
	Examiner	Art Unit	
	DUC Q. DINH	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *personal interview with applicant's representative on 10/21/08*.

2. ☒ The allowed claim(s) is/are *1-5 and 11-14*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 09/29/03,12/10/06
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

/Duc Q Dinh/
Primary Examiner, Art Unit 2629

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Applicant's Representative, Hosang Lee on October 21, 2008.

The application has been amended as follows:

1. (Currently Amended) A liquid crystal display comprising:

a liquid crystal panel having a large number of picture elements arranged at intersections of plural selection lines and data lines;

a selection line signal output IC for outputting a selection line signal to the selection lines of said liquid crystal panel;

a reference voltage generator circuit, which comprises first resistors connected in series between two voltages and second resistors connected in series to said first resistors, generates plural reference voltages from respective connection points of the first resistors, switches over the reference voltage either to an image display voltage or to a black display voltage, and outputs the switched reference voltage to plural wiring lines connected to the connection points; and

a signal line drive IC, to which an image data signal and the reference voltage are inputted, and which outputs a voltage based on the reference voltage and the image data signal, to a data line of the liquid crystal panel,

wherein the reference voltage generator circuit has a switch section which is opened and closed by a black voltage selection signal, and

the switch section has first switching element[[s]] arranged in parallel to the first ~~registers~~ resistors so as to open and close between a connection point for generating a black voltage and a connection point for generating a white voltage among the plural image display voltages, and second switching element[[s]] which [[are]] is arranged so as to control resistance values of the second resistors and output value of which [[have]] has ~~polarities~~ opposite polarity to [[those]] output value of the first switching element[[s]], and outputs a black display voltage to the plural wiring lines by turning the first switching element[[s]] into closed states, and turning the second switching element[[s]] into opened states, on the basis of the black voltage selection signal to short-circuit between the connection points and to change resistance values of the second resistors, and

the signal line drive IC outputs a black write voltage to the data line on the basis of the black display voltage, and

the switch section includes an image display period for supplying said image display voltage and a black display period for supplying the black display voltage in one horizontal period, and is switched over by the black voltage selection signal, so as to be synchronized with a change of a selection line signal in a row of the selection line for writing an image therein and a row thereof for writing black therein.

2. (Previously Presented) The liquid crystal display according to claim 1, wherein when said selection line signal output IC drives nG selection lines and a selection line clock period TH is used for driving said selection lines, a signal, which

makes the output of said selection line signal output IC valid when said reference voltage is switched to the image display voltage while making the output of said selection line signal output IC invalid when said reference voltage is switched to the black display voltage, is inputted to said selection signal output IC during nGTH period from input of a start pulse, and an inverted signal of said signal is inputted after the nGTH period.

3. (Previously Presented) The liquid crystal display according to claim 1, wherein said reference voltage is switched from the black display voltage to the image display voltage at time T1 and switched from the image display voltage to the black display voltage at time T2, said selection line signal output IC outputs the selection line signals so that the lines of the selection lines selected at time (T2-T1)/2+T1 are changed to a non-selective state at a time later than (T2-T1)/2+T1 and earlier than T2.

4. (Previously Presented) The liquid crystal display according to claim 1, wherein said reference voltage is switched in a period during which no image data is loaded in said signal line drive IC.

5. (Original) The liquid crystal display according to claim 1, wherein said reference voltage is switched during a period when image data are loaded in said signal line drive IC.

6-10. (Canceled)

11. (Currently Amended) A liquid crystal display comprising:

a liquid crystal panel having a large number of picture elements arranged at intersections of plural selection lines and data lines;

a selection line signal output IC for outputting a selection line signal to the selection lines of said liquid crystal panel;

a reference voltage generator circuit, which comprises first resistors connected in series between two voltages and second resistors connected in series to said first resistors, generates plural reference voltages from respective connection points of the first resistors, and outputs them to plural wiring lines connected to the connection points as image display voltages, and a signal line drive IC, to which an image data signal, a control signal and the reference voltage generated by the reference voltage generator circuit are inputted, and which outputs an image write voltage based on the image display voltage, to a data line of the liquid crystal panel,

wherein the reference voltage generator circuit has a switch section which is switched over, by a black voltage polarity selection signal, either to a first reference voltage generation mode in which the black display voltage is always generated under positive polarity and the image display voltage is generated under negative polarity or a second reference voltage generation mode in which the black display voltage is always generated under negative polarity and the image display voltage is generated under positive polarity, and

the switch section has first switching element[[s]] arranged in parallel to the first ~~registers~~ resistors so as to short-circuit a connection point for generating a black voltage

and a connection point for generating a white voltage among the plural image display voltages, and second switching element[[s]] which [[are]] is arranged so as to control resistance values of the second resistors and output value of which have opposite polarity ~~polarities~~ to [[those]] output value of the first switching element[[s]], and outputs a black display voltage to the plural wiring lines by turning the first switching element[[s]] into closed states, and turning the second switching element[[s]] into opened states, on the basis of the black voltage selection signal to short-circuit between the connection points and to change resistance values of the second resistors, on the basis of the black selection signal, in the positive polarity and negative polarity respectively, and

the signal line drive IC outputs a black write voltage to the data line on the basis of the black display voltage, and the first reference voltage generation mode and the second reference voltage generation mode are alternatively switched over every vertical period by the black voltage polarity selection signal, so that said image write voltage or said black write voltage is outputted during one vertical period, about the picture element

12. (Previously Presented) The liquid crystal display according to claim 11, wherein said reference voltage generator circuit is comprised of resistors connected in series, and said resistance values are changed by switching elements connected in series or in parallel to said resistors.

13. (Previously Presented) The liquid crystal display according to claim 11, wherein said reference voltage generator circuit is comprised of a semiconductor device

capable of inputting a digital signal, and a voltage of an arbitrary value is generated conforming to said digital signal.

14. (Previously Presented) The liquid crystal display according to claim 1, wherein the switch section is formed by analog switches.

Allowable Subject Matter

2. Claims 1-5 and 11-14 are allowed.

Reason for Allowance

3. The following is an examiner's statement of reasons for allowance:

The present invention related to a . Each independent claim identifies the uniquely distinct features " ".

As per claim 1,

wherein the reference voltage generator circuit has a switch section which is opened and closed by a black voltage selection signal, and

the switch section has first switching element arranged in parallel to the first – resistors so as to open and close between a connection point for generating a black voltage and a connection point for generating a white voltage among the plural image display voltages, and second switching element which is arranged so as to control resistance values of the second resistors and output value of which has opposite polarity to output value of the first switching element[, and outputs a black display voltage to the plural wiring lines by turning the first switching element[[s]] into closed states, and turning the second switching element into opened states, on the basis of the

black voltage selection signal to short-circuit between the connection points and to change resistance values of the second resistors.

In reference to claim 11,

the switch section has first switching element[arranged in parallel to the first – resistors so as to short-circuit a connection point for generating a black voltage and a connection point for generating a white voltage among the plural image display voltages, and second switching element which is arranged so as to control resistance values of the second resistors and output value of which have opposite polarity – to output value of the first switching element, and outputs a black display voltage to the plural wiring lines by turning the first switching element into closed states, and turning the second switching element into opened states, on the basis of the black voltage selection signal to short-circuit between the connection points and to change resistance values of the second resistors, on the basis of the black selection signal, in the positive polarity and negative polarity respectively.

4. The closest prior arts of Nose et al. (U.S Patent No. 6,819,311) and Kudo et al. (U.S Patent No. 6,781,605) show similar systems, but either singularly or in combination, fail to anticipate or render above quoted limitations obvious.

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled “Comments on Statement of Reasons for Allowance.”

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DUC Q. DINH whose telephone number is (571)272-7686. The examiner can normally be reached on Mon-Fri from 8:00.AM-4:00.PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RICHARD HJERPE can be reached on (571)272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Duc Q Dinh/
Primary Examiner, Art Unit 2629